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EXAMINER
RUGGLES, JOHN S

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 09/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/066,849	Applicant(s) LEE ET AL.
	Examiner John Ruggles	Art Unit 1756

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2002 and 04 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *15-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1-14* is/are objected to.

8)☒ Claim(s) *1-20* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14, drawn to a manufacturing method, classified in class 430, subclass 312.

II. Claims 15-20, drawn to a semiconductor device, classified in class 257, subclass 798.

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process can be used to make another and materially different product, such as an integrated circuit which is not an active semiconductor device.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Michael Hull on 8 July 2003 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-14. Affirmation of this election must be made by applicant in replying to this Office action. Claims 15-20 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

The drawings are objected to because: Figure 3D shows the width d_2 of the trench in the trench mask 42 to be ***wider*** than that of the underlying via hole in the third interlayer insulating layer 36, while the description of this figure found at line 1 on page 8 of the specification refers to this width d_2 as "narrower" than that of the underlying via hole. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because it does not match the written description and drawings filed therewith. Specifically, the abstract leaves out any mention of third and fourth interlayer insulating layers 36 and 41, respectively, as shown in Figures 3B-3E and described from page 6, line 5 through page 8, line 18. Also, the abstract refers to formation of a "first interlayer insulating layer" on the "first interconnection line", presumed to mean element 35, as shown in these figures. This suggests that the first interlayer insulating layer found in the abstract is actually a reference to the "third interlayer insulating layer" 36 found elsewhere in the specification, as pointed out above. In order to make this correspondence clear, applicant should either describe each layer with the same name as is disclosed in the specification, or at least include unique reference numbers next to such layers in the abstract to allow correlation of these layers with the instant figures and their corresponding portions of the written description. Correction is required. See MPEP § 608.01(b).

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is replete with terms, which are not clear, concise and exact. The specification should be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: (1) at line 6 on page 2, "upper and interconnection lines" should be changed (e.g., to --upper and lower interconnection lines--, etc.), in order to parallel the similar phrase "lower and upper interconnection lines" found on page 1 at line 21; (2) at line 32 on page 3, "is occurred" should be corrected to --occurs--, to be grammatically correct; (3) at line 14 on page 8, the fourth interlayer insulating layer "36" must be corrected to --41--, as described earlier at line 5 on this same page, and also in order to correspond to Figure 3E; (4) at line 16 on page 8, --and-- has been misspelled; (5) at lines 29-32, also on page 8, "The diffusion barrier layer...deposited" is an incomplete sentence; and (6) the second paragraph found on page 9 at lines 6-11 is confusing and must be rewritten to clearly set forth the purpose for applicants' invention, as supported by the originally filed disclosure. Note that due to the number of errors, those listed here are merely *examples* of the corrections needed and do *not* represent an exhaustive list thereof.

Appropriate correction is required. An amendment filed making all appropriate corrections must be accompanied by a statement that it contains no new matter.

Claim Objections

Claims 1-14 are objected to because of the following informalities: (1) in claim 1 at line 4 on page 10, "of semiconductor device" should be changed to --of a semiconductor device--, to be grammatically correct and at line 19 on page 10, "etching stop pattern" should be changed to -

-etching stop patterns--, to match this phrase found earlier at line 15 on page 10 and (2) in (a) claim 7 at line 29 on page 11, "plasma enhance chemical vapor deposition method" should be corrected to --plasma enhanced chemical vapor deposition-- and similarly in (b) claim 9 (at line 8 on page 12) and (c) claim 11 (at line 20 on page 12), "enhance" should be corrected to --enhanced--, to be grammatically correct in all three instances. Claims 2-14 are dependent on claim 1. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-14 are unclear with regard to the order in which the different layers are formed, especially when compared to the instant figures and their corresponding descriptions. For example, at lines 5-14 on page 10 claim 1 recites forming a "first interconnection line" on a semiconductor substrate, a "first interlayer insulating layer" thereon, followed by a "first etching stop layer" thereon, then forming a via hole by etching through the first etching stop layer and the first interlayer insulating layer to expose the underlying first interconnection line. However, this sequence of steps appears to best correlate to instant Figure 3B as described in the specification, if the claimed (a) "first" interlayer insulating layer and (b) "first" etching stop layer are interpreted to mean (a) the "third interlayer insulating layer" 36 found at lines 5-6 on page 6

and (b) the second "etching stop layer" 37 found at line 7, also on page 6, respectively. This lack of clarity is compounded by claim 3 at lines 4-9 on page 11, in which the (c) "third interlayer insulating layer" and (d) "second etching stop layer" appear to best correlate to previously formed (c) second "interlayer insulating layer" 33 and (d) first "etching stop layer" 34, respectively, both found at lines 27-33 on page 5 of the specification in reference to Figure 3A. Further, in claim 8 at line 3 on page 12, the thickness of the "second interlayer insulating layer" recited as "about 3,000 Å to about 30,000 Å" is interpreted in light of the disclosure to instead mean --about 2,000 Å to about 30,000 Å--, based on the range found at line 27 on page 7 for the "fourth interlayer insulating layer" 41, which seems to be best correlated to this recited layer. Similarly, in claim 10 at line 15 on page 12, the thickness of the "first interlayer insulating layer" recited as "about 2,000 Å to about 30,000 Å" is interpreted in light of the disclosure to instead mean --about 3,000 Å to about 30,000 Å--, based on the range found at line 26 on page 6 for the "interlayer insulating layer" 36, which seems to be best correlated to that recited layer. Claims 2-14 are dependent on claim 1. Applicants' assistance is required in rewriting claim 1 and all appropriate dependent claims to properly correlate with the instant figures and their written descriptions, as originally filed. This can be done by either (1) using the same language in the claims as is found in the specification and/or (2) inserting the applicable figure element numbers in the claims (in parentheses, in order to avoid an objection in accordance with MPEP § 608.01(m)).

Claim 7 at line 28 on page 11 lacks antecedent basis for "the high density plasma".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent 6,093,632) in view of Lin, et al. (US Patent 6,042,999).

Lin '632 teaches a modified dual damascene method for manufacturing multi-level interconnection lines in a semiconductor device. The method involves forming conductive (copper, Cu, instant claim 13) interconnection lines 2 in a first (1^{st}) insulator (silicon oxide) 1, which is understood to be on a semiconductor substrate. Layers 1 and 2 are covered by a 1^{st} etching stop layer 3 (silicon nitride, instant claim 3), a second (2^{nd}) insulator (silicon oxide) 4 formed by either plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD) to 4,000-15,000 Å thick (column 4, lines 6-9, instant claims 9-10), and a 2^{nd} etching stop layer 10a (silicon nitride 200-2,000 Å thick by e.g., PECVD, etc., column 5, lines 25-27, instant claims 11-12), as shown in Figure 4 (column 5, lines 18-28). A resist pattern 11 is used as an etching mask to pattern narrow openings 12a for via holes in the 2^{nd} etching stop layer 10a, to form a patterned etching stop layer 10b, as shown in Figure 5 (column 5, lines 29-43). After removing the resist, the patterned etching stop layer 10b is covered by a third (3^{rd}) insulator layer 13 (silicon oxide by e.g. PECVD, etc. to about 3,000-

15,000 Å thick), followed by forming another patterned resist mask 14, having wider openings 15a for forming wide trenches connecting over the narrow via holes, as shown in Figure 6 (column 5, lines 43-53, instant claim 5). The wide trenches and narrow via holes are etched through the resist mask 14 and etching stop pattern portions 10b through the insulators 13 and 4 and etching stop layers 10b and 3 down to the conductive interconnection lines 2, as shown in Figure 7 (column 5, line 54 to column 6, line 8, instant claim 4). A conductive layer 16 is formed to fill the trenches and connected underlying via holes onto the tops of conductive lines 2, as shown in Figure 8 (column 6, lines 9-29, instant claims 1-2). While not specifying the thickness of the Cu conductive interconnection lines 2, the figures suggest this thickness is similar to those of insulator layers 3 and 13 (or about 3,000-15,000 Å thick, instant claim 14). Lin '632 patterns the etching stop layer to leave only small area islands 10b, in order to reduce or limit increase in capacitance usually caused by wider area etching stop layers (column 2, lines 15-25). Also, while the teachings of Lin '632 are described in terms of this method as a preferred embodiment, it is understood by those skilled in the art of dual damascene multi-level interconnection manufacture of semiconductor devices that various changes may be made in the details of this embodiment without departing from the spirit and scope of these teachings (column 6, lines 36-40).

While teaching a dual damascene method for manufacturing multi-level interconnection lines similar to the instant invention, Lin '632 does not specify forming the via holes before forming the patterned etching stop patterns around the via inlets and subsequent trench patterning of the overlying 3rd insulator layer.

Lin '999 shows a robust dual damascene method of manufacturing multi-level interconnection lines in a semiconductor device that involves formation of a via 145, before forming an overlying trench 165, as shown in Figures 2b and 2f (column 5, line 20 to column 6, line 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have changed the order of steps in the embodiment described by Lin '632 so as to form via openings before forming the patterned etching stop layer portions 10b, then overlying and patterning the 3rd insulator layer to form trenches therein. This is because Lin'632 suggests changes to the details of his preferred embodiment without departing from the spirit and scope of those teachings relating to use of patterned reduced area islands of etching stop material to reduce capacitance under that which would have resulted if a wider area etching stop layer had been used. Also, formation of via holes followed by subsequent formation of trenches over these via holes (via first, rather than trench first) is already known in dual damascene semiconductor device manufacture, as shown by Lin '999.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin '632 in view of Lin '999 and further in view of Huang (US Patent 6,268,283).

Huang describes a dual damascene method for manufacturing multi-level interconnects in a semiconductor device (column 1, lines 1-11). The method includes etching through a patterned resist 212 to form a via hole 214 through a hard mask 210, a dielectric 208, and etching stop layers 206 and 204 down to an interconnecting conductor 202, as shown in Figure 2B (column 3, lines 29-32). After removing remaining resist 212, a cap layer 216 is formed over the hard mask

210, covering the top region 218 of via hole 214 and leaving a void in the lower region of the via hole 214, as shown in Figure 2C (instant claim 6). The cap layer 216 (e.g., silicon oxide, silicon nitride, silicon oxynitride, etc., preferably formed by PECVD to a thickness of 1,000-2,000 Å, instant claims 7-8) supports a subsequent overlying resist having a trench pattern 224 and also prevents low-level devices or layers (e.g., dielectric layers 208 and 204, etc.) from being damaged during developing of the resist (column 3, lines 33-56). The cap layer 216, the hard mask 210, and the dielectric 208 are then etched using the patterned resist 224 as an etching mask to form a trench 226, as shown in Figure 2D (column 3, lines 57-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a cap layer to form a void within the via hole as described by Huang in the dual damascene method taught by Lin '632 and shown by Lin '999 in order to support an overlying resist pattern and protect lower-level devices and layers as described by Huang and also because all three references relate to the same art of dual damascene manufacture of multi-level interconnects in semiconductor devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 703-305-7035. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 703-308-2464. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

John Ruggles
Examiner
Art Unit 1756

MARK F. HUFF
SUPERVISORY PATENT EXAMINER
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